What is claimed is:

1. A semiconductor integrated circuit for generating an output control signal for controlling output of stored data, including:

output control signal generating means for delaying in parallel, by using a read command internal signal, an internal clock corresponding to an external clock received from external and the inverted internal clock, respectively, and counting the internal clock and the inverted internal clock with delay times different from each other, to output an output control signal.

2. The semiconductor integrated circuit as recited in claim 1, wherein the output control signal generating unit includes:

internal clock delaying means for outputting a plurality of delayed internal clocks having delay times different from each other by using the received internal clock;

internal clock edge detecting means for subsequently counting, after counting the first delayed internal clock among the plurality of the delayed internal clocks by using the read command internal signal, the other delayed internal clocks among the plurality of delayed internal clocks than the first delayed internal clock;

inverted internal clock delaying means for outputting a plurality of delayed inverted internal clocks having delay

times different from each other by using the received inverted internal clock; and

inverted internal clock edge detecting means for subsequently counting, after counting the first delayed inverted internal clock among the plurality of the delayed inverted internal clocks by using a signal outputted from the internal clock edge detecting means, the other delayed inverted internal clocks among the plurality of the delayed inverted internal clocks than the first delayed inverted internal clock.

3. The semiconductor integrated circuit as recited in claim 2, wherein the internal clock delaying means includes a plurality of delaying circuits coupled in parallel to each other for outputting the plurality of the delayed internal clocks.

4. The semiconductor integrated circuit as recited in claim 3, wherein the delay times of the plurality of the delaying circuits include the delay time between the external clock and the internal clock.

5. The semiconductor integrated circuit as recited in claim 4, wherein the delay time of the first delaying circuit for outputting the first delayed internal clock further includes the delay time from the read command to generation of the read command internal signal.

6. The semiconductor integrated circuit as recited in claim 5, wherein the internal clock edge detecting means includes a plurality of internal clock edge detecting means, at least coupled to the outputs of the plurality of the delaying circuits, respectively, for subsequently counting the outputs from the plurality of the delaying circuits.

7. The semiconductor integrated circuit as recited in claim 6, wherein one of the plurality of the internal clock edge detecting means receives the output signal from another one of the plurality of the internal clock edge detecting means and counts the internal clock at the initial rising edge of the internal clock that exists after the output signal.

8. The semiconductor integrated circuit as recited in claim 2, wherein the inverted internal clock delaying means includes a plurality of delaying circuits coupled in parallel to each other for outputting the plurality of the delayed inverted internal clocks.

9. The semiconductor integrated circuit as recited in claim 8, wherein the inverted internal clock edge detecting means includes a plurality of inverted internal clock edge detecting means, at least coupled to the outputs of the plurality of the delaying means, respectively, for

subsequently counting the outputs of the plurality of the delaying circuits.

10. The semiconductor integrated circuit as recited in claim 9, wherein one of the inverted integral clock edge detecting means receives the output signal from another one of the plurality of the inverted internal clock edge detecting means and counts the inverted internal clock at the initial rising edge of the inverted internal clock that exists after the output signal.

11. The semiconductor integrated circuit as recited in claim 1, wherein the output control signal generating unit includes:

internal clock delaying means for outputting a plurality of delayed internal clocks having delay times different from each other by using the received internal clock;

internal clock edge detecting means for subsequently counting, after counting the first delayed internal clock among the plurality of the delayed internal clocks by using the read command internal signal, the other delayed internal clocks among the plurality of the delayed internal clocks than the first delayed internal clock;

inverted internal clock delaying means for outputting a plurality of delayed inverted internal clocks having delay times different from each other by using the received inverted internal clock; and

inverted internal clock edge detecting means for subsequently counting, after counting the first delayed inverted internal clock among the plurality of the delayed inverted internal clocks by using the read command internal signal, the other delayed inverted internal clocks among the plurality of the delayed inverted internal clocks than the first delayed inverted internal clock.

12. The semiconductor integrated circuit as recited in claim 11, wherein the internal clock delaying means includes a plurality of delaying circuits coupled in parallel to each other for outputting the plurality of the delayed internal clocks.

13. The semiconductor integrated circuit as recited in claim 12, wherein the delay times of the plurality of the delaying circuits include the delay time between the external clock and the internal clock.

14. The semiconductor integrated circuit as recited in claim 13, wherein the delay time of the first delaying circuit for outputting the first delayed internal clock further includes the delay time from the read command to generation of the read command internal signal.

15. The semiconductor integrated circuit as recited in claim 12, wherein the internal clock edge detecting means

includes a plurality of internal clock edge detecting means, at least coupled to the outputs of the plurality of the delaying circuits, respectively, for subsequently counting the outputs from the plurality of the delaying circuits.

16. The semiconductor integrated circuit as recited in claim 15, wherein one of the plurality of the internal clock edge detecting means receives the output signal from another one of the plurality of the internal clock edge detecting means and counts the internal clock at the initial rising edge of the internal clock that exists after the output signal.

17. The semiconductor integrated circuit as recited in claim 11, wherein the inverted internal clock delaying means includes a plurality of delaying circuits coupled in parallel to each other for outputting the plurality of the delayed inverted internal clocks.

18. The semiconductor integrated circuit as recited in claim 17, wherein the inverted internal clock edge detecting means includes a plurality of inverted internal clock edge detecting means, at least coupled to the outputs of the plurality of the delaying means, respectively, for subsequently counting the outputs of the plurality of the delaying circuits.

19. The semiconductor integrated circuit as recited in claim 18, wherein one of the inverted integral clock edge detecting means receives the output signal from another one of the plurality of the inverted internal clock edge detecting means and counts the inverted internal clock at the initial rising edge of the inverted internal clock that exists after the output signal.

20. An output control signal generating method for generating an output control signal for controlling output of stored data, the method comprising the steps of:

(a) outputting a plurality of delayed internal clocks having delay times different from each other by using a received internal clock;

(b) subsequently counting, after counting the first delayed internal clock among the plurality of the delayed internal clocks by using a read command internal signal, the other delayed internal clocks among the plurality of the delayed internal clocks than the first delayed internal clock;

(c) outputting a plurality of delayed inverted internal clocks having delay times different from each other by using the received inverted internal clock; and

(d) subsequently counting, after counting the first delayed inverted internal clock among the plurality of the delayed inverted internal clocks by using the signal outputted at the step (b), the other delayed inverted

internal clocks among the plurality of the delayed inverted internal clocks than the first delayed inverted internal clock.

21. The output control signal generating method as recited in claim 20, wherein one of the plurality of the delayed internal clocks at the step (a) includes a delay time between the external clock and the internal clock and a delay time from the read command to generation of the read command internal signal.

22. The output control signal generating method as recited in claim 21, wherein the step (b) includes a plurality of internal clock edge detecting means for at least receiving and subsequently counting the plurality of the delayed internal clocks, respectively.

23. The output control signal generating method as recited in claim 22, wherein one of the plurality of the internal clock edge detecting means receives the output signal from another one of the plurality of the internal clock edge detecting means and counts the internal clock at the initial rising edge of the internal clock that exists after the output signal.

24. An output control signal generating method for generating an output control signal for controlling output of

stored data, the method includes the steps of

(a) outputting a plurality of delayed internal clocks having delay times different from each other by using the received internal clock;

(b) subsequently counting, after counting the first delayed internal clock among the plurality of the delayed internal clocks by using a read command internal signal, the other delayed internal clocks among the plurality of the delayed internal clocks than the first delayed internal clock;

(c) outputting a plurality of delayed inverted internal clocks having delay times different from each other by using the received inverted internal clock; and

(d) subsequently counting, after counting the first delayed inverted internal clock among the plurality of the delayed inverted internal clocks by using the read command internal signal, the other delayed inverted internal clocks among the plurality of the delayed inverted internal clocks than the first delayed inverted internal clock.

25. The output control signal generating method as recited in claim 24, wherein one of the plurality of the delayed internal clocks at the step (a) includes a delay time between the external clock and the internal clock and a delay time from the read command to generation of the read command internal signal.

26. The output control signal generating method as

recited in claim 25, wherein the step (b) includes a plurality of internal clock edge detecting means for at least receiving and subsequently counting the plurality of the delayed internal clocks, respectively.

27. The output control signal generating method as recited in claim 26, wherein one of the plurality of the internal clock edge detecting means receives the output signal from another one of the plurality of the internal clock edge detecting means and counts the internal clock at the initial rising edge of the internal clock that exists after the output signal.